

Teaching Hardware Description and Verification

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Course Aims

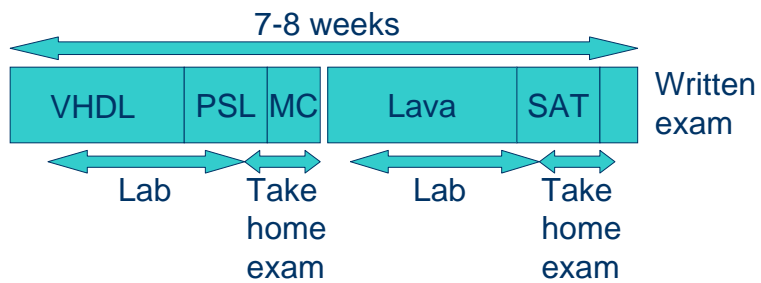
Give insights into state of the art hardware design and verification methods.

Relevant both for industrial applications and current research.

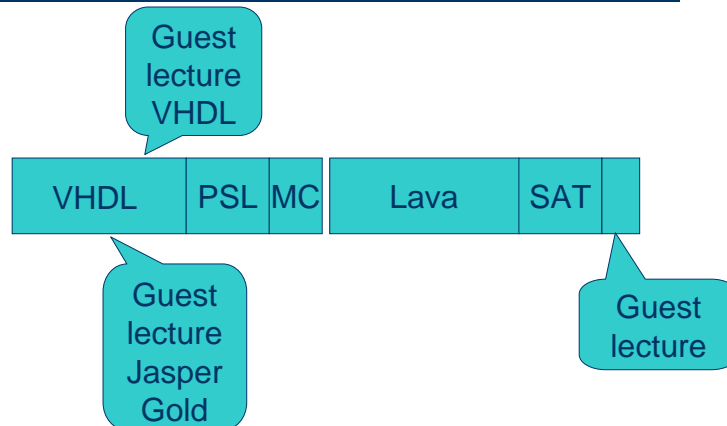
Course Outline



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Gaisler's VHDL style

- o Helps guide students to design their own code
- o Separates the flip flops from the logic by using two processes per entity:

Sequential process

- Sensitive to clock (and asynchronous reset)
- Handles internal flip flops (copies the next value to the current)

Combinational process

- Sensitive to input signals and current values of flip flops
- Calculates values of all output ports, and the next values of flip flops

Property Specification Language, PSL

- Standardised by Accellera
- Used by the Jasper Gold tool
- Both branching and linear time logic

```
property fifo_no_write_error is
    always (not full -> next (not wr_err));

property req_ack is
    {[*],req} | => {!ack[4], ack};
```

Lava

- Hardware description language embedded in the lazy functional language Haskell
- Example: Sklansky parallel prefix circuit

```
sklansky op [a] = [a]
sklansky op as = (sklansky op >|> join op (sklansky op)) as
  where join op f (a:as) = withEach op (a: f as)
```



32 lines, 5 stages, 17 max fanout, horizontal wirelength is 49, 80 operators.

Course Literature

- Ashenden: Designer's Guide to VHDL (book)
- Claessen & Sheeran: Lava Tutorial
- Seger: An Introduction to Formal Hardware Verification
- Hu: Formal Hardware Verification with BDDs: An Introduction
- Kern & Greenstreet: Formal Verification in Hardware Design: A Survey

Guest Lecturers over the Years

- **Intel:** John Harrison, Carl-Johan Seger, Richard Sharp
- **Xilinx:** Satnam Singh, Göran Bilski
- **Synopsys:** Per Bjesse
- **Jasper Design Automation / Safelogic:** Øystein Kolsrud, Johan Alfredsson
- **Prover Technology:** Henrik Persson
- **Gaisler Research:** Jiri Gaisler
- **Chalmers:** Koen Claessen, Per Larsson-Edefors

Two halves: Why and How

- Prepare the students for both industry and academia
- Different views complement each other
- Similar assignments in both halves makes solutions simpler, and offers an opportunity to compare the approaches

Advantages for the Research Group

- Forces us to keep up with trends in industry
- Gives us natural contacts with industry
- A source of good masters thesis students
- Motivation to develop new case studies and documentation for our own tools (with quick feedback)

Conclusions

- We teach both VHDL and Lava
- The course has lead to closer contacts with industry
- The course stimulates our research