

## SESSION 3 – SYSTEM LEVEL DESIGN

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**Session Chair:**

*Don Bouldin, University of Tennessee*

**Speakers:**

*Reiner Hartenstein, Univ/ of Kaiserslautern*

*Carsten Bieser, University of Karlsruhe*

*Joe Schneider, Iowa State University*

2005 Microelectronic Systems Education Conference

## *Reiner Hartenstein*

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- Dr. Reiner Hartenstein is currently Professor of Computer Science and Engineering at the Technical University of Kaiserslautern in Germany. He received all of his degrees from the E.E. Dept. at Karlsruhe University.
- He is known world-wide for his advocacy of computer architectures that do not follow the traditional von Neumann paradigm including the Xputer and reconfigurable arrays.
- He is a founder of FPL (Field Programmable Logic) which will be held 24-26 Aug. 2005 in Tampere, Finland.
- Dr. Hartenstein is a IEEE Fellow.

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## *Carsten Bieser*

- Mr. Bieser is a Ph.D. student at Karlsruhe University, having completed his M.S. degree there in 2001.
- His research involves rapid prototyping of automotive systems and embedded system design.
- He is responsible for the Design Automation Lab.
- His advisors and co-authors are Professors Mueller-Glaser and Becker.

*Hardware/Software Co-Training Lab:  
From VHDL Bit-Level Coding up to CASE-Tool based System Modelling*

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## *Joe Schneider*

- Mr. Schneider is a M.S. student at Iowa State University, having completed his B.S. degree at North Dakota State.
- His research involves accurate modeling and profiling of FPGA systems in system-level design languages.
- His co-authors are Mikel Bezdek, Ziyu Zhang, Zhao Zhang and Prof. Diane Rover.

*A Platform FPGA-based Hardware-Software Undergraduate Laboratory*

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