


Simplifying Analog CMOS Design for Undergraduates

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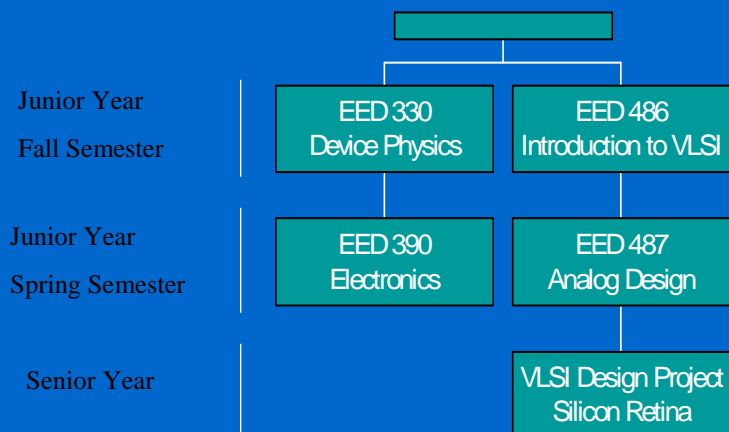
Outline of Talk

- Reasons for Analog design for undergraduates
 - Details of the curriculum in VLSI at Alfred and examples of projects
 - Details of the Analog course
 - Description of projects in Analog for undergrads
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Trends in Teaching VLSI Design to Undergraduates

- VLSI design methodology includes partitioning, testing, time to market, design for testing, etc.
- Many of today's applications require analog and mixed-mode solutions.
- New technologies such as HDLs or FPGAs are often offered as separate courses.

VLSI Design Curriculum at Alfred



OUTLINE OF VLSI PROJECTS

- Systems level
 - Verilog HDL or schematic entry
 - Implemented as standard cells or FPGAs.
- Analog-Sampling Circuits
 - Physical level design-SPICE simulated and verified-some heirarchial design
- Mixed mode-Silicon Retina

Advantages of teaching Analog design to undergraduates

- Prepares them for advanced study in industry or academia
- *analog design includes the basic principles of fabrication, device physics and physical layout that would not have to be included in an introductory digital VLSI course,*
- *A good background in analog design will prepare a student for more advanced VLSI courses.*

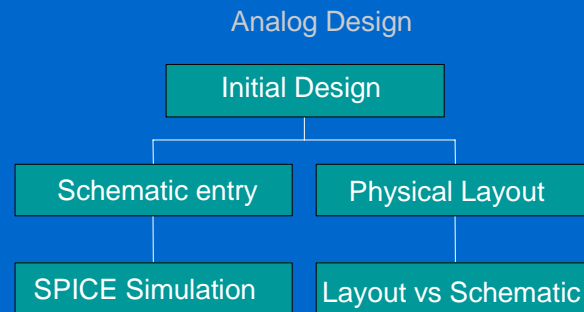
Disadvantages of Teaching Analog design

- Theory can be tedious for undergraduates
- Labs are time consuming
- Projects can be boring
- Students get bogged down drawing transistors

Analog Design, EED487

- Details of VLSI physical layout, including Device physics, fabrication, and SPICE extraction and simulation, are covered in the Analog design course. Laboratories for the course at Alfred include the following:
 1. Two transistor current mirror.
 2. Fifteen transistor operational amplifier
 3. Sampling circuit, such as sc circuit.
- Includes design, simulation, layout, verification, and testing.

Physical Design Process



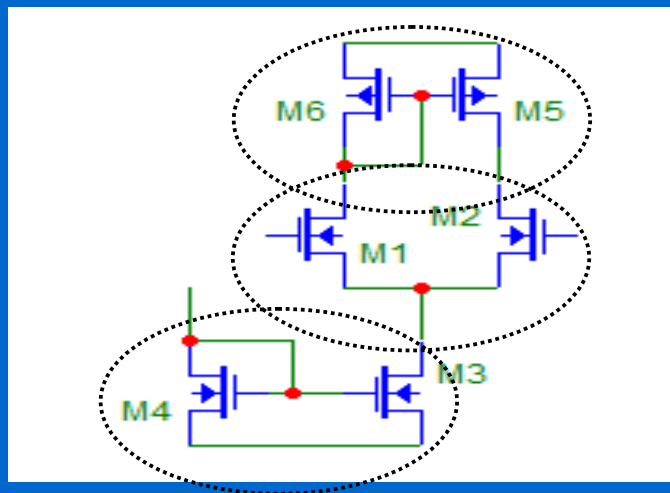
Design Paradigm for Layout of an opamp

- Three step process
 - matched pair.
 - common factor
 - common centroid
- Matched pair-Look for optimum symmetry in the design.
 - Matched pair to minimize distributed RC effects

Common Factor

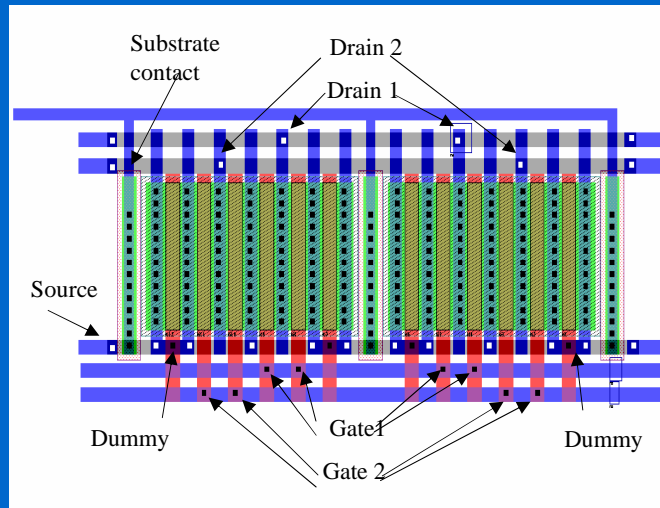
- Design aspect ratios around a common factor, usually 4, 8 or 12.
- Identify Matched pairs of the design.
- Construct a "cell library" of matched pair parts that are easily constructed from one or two central cells.
- Use an autorouter to route the cells.

Example: Simple stage of op-amp

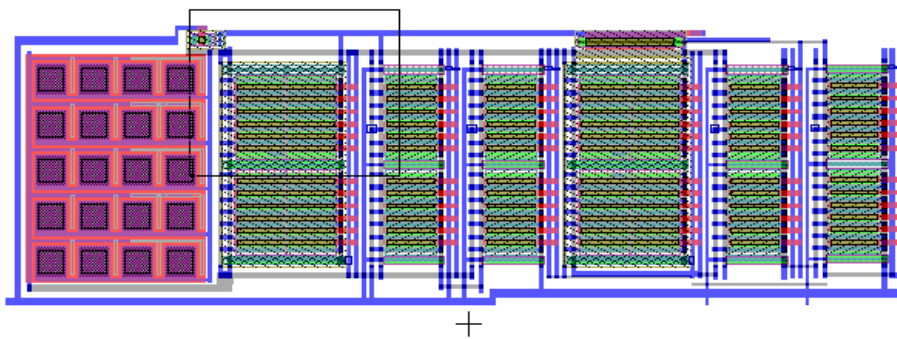


Stack generator matched pair

R. Naiknaware and T. Fiez *IEEE JSSC* 34 (3) 1999



Idealized result



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Layout Issues Concerning Analog VLSI- Advantages of the Stack Cell approach

- Objective: speed up analog design time.
- As possible support for Analog Hierarchical design. (Stack generators).
- For reducing effects of topographical process gradients. (Film thickness, over-etching, etc). and temperature gradients

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Problems with testing

- If the course includes MOSIS fabrication, Seniors have left the institution by the time chips are fabricated.
- For the course, students test last years chips
- Parts fabricated are tested when they return from MOSIS in the fall by juniors taking the course

Testing includes

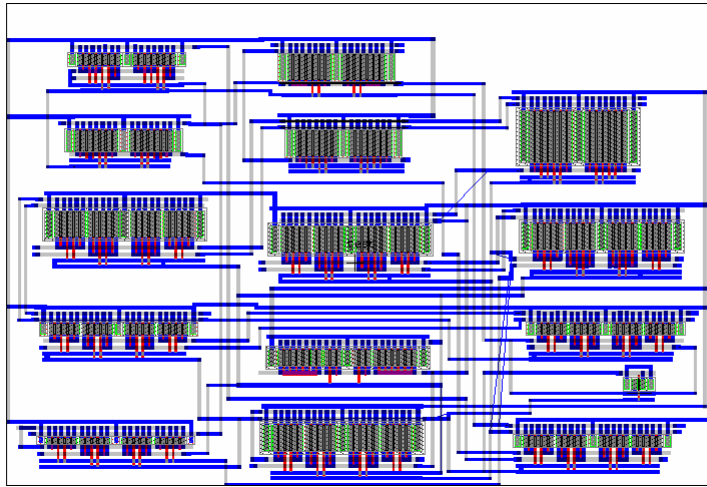
- Bench tests of current sources, opamps and sc circuits

Summary

Alfred University

- VLSI comes in two basic flavors: HDL synthesis and Analog.
- Some industrial and some graduate level work but mostly Undergraduate.
- Stack cell approach saves time in layout of analog design

Autorouted Folded Cascode Layout



Use Stack Generation to minimize noise and offsets

