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## A New Hardware/Software Codesign Environment and Senior Capstone Project for Computer Engineering

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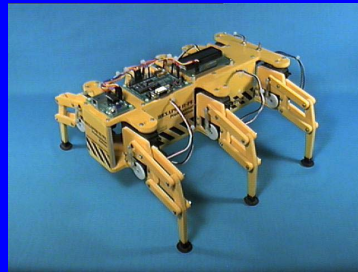
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## The Past - Advanced Digital Design Capstone Project

- Project is based on based on a commercial hobby robot chassis - the Hexapod II from Lynxmotion (<http://www.lynxmotion.com>)
- Six-legged robot was chosen to provide more of a challenging control problem than a simple wheeled robot
- A microcontroller is used to perform the "higher-level" functions and a custom digital IC is used to perform the basic control functions
- Additional hardware is necessary to generate servo positioning pulses within specified time limits



Servo position controlled by pulse width of 0.5 ms to 2.5 ms

Pulses (regardless of size) must repeat at 10 ms intervals





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## CCLI Project Goals



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- Introduce computer engineering students to the theory and practice of system-level modeling and design
  - performance modeling and architecture selection
  - hardware/software partitioning, codesign, and coverification
- Development of:
  - an easy-to-use, freely available performance modeling tool that students can use to examine the effects of architectural tradeoffs
  - a library of hardware/software communications mechanisms so that students can concentrate on the system-level architecture and design
  - example projects that incorporate the use of the tools in the design of hardware/software systems
  - lecture and laboratory material to support the teaching of system design concepts



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## Performance Based Modeling Tool *PBMT*

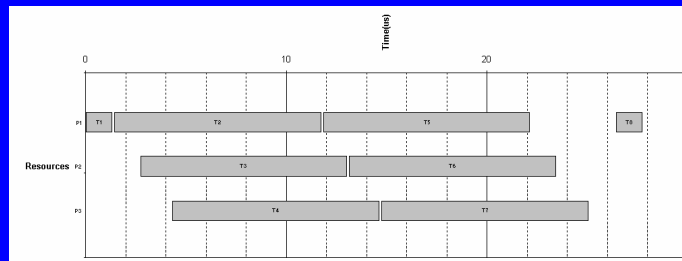
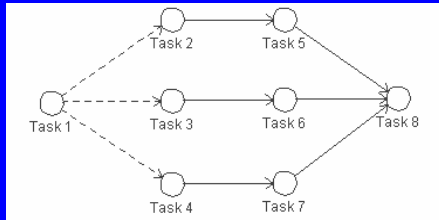


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- Abstract-level performance modeling tool designed to be used in undergraduate classes and for student design projects
  - simple to understand and apply to student-type designs
  - have a significant level of “prefabrication” to ease model development effort and time
  - as application and implementation independent as possible
  - portable, easy to install, and low- or no-cost
    - standard languages, e.g., SystemC, VHDL, Java



# PBMT



# Hardware/Software Communications Library



- Designed to free students from having to develop low-level bus protocols for communicating between hardware and software
  - Allows students to concentrate on the HW/SW architecture and achieving the overall project objective
  - At the senior level, most students have sufficient experience in low-level digital design, but not in system level design issues
- Each communications library module includes a software API (C, C++), synthesizable VHDL to implement the hardware portion, and a datasheet covering the function and use of the module
- Examples include:
  - memory mapped, non-blocking, single word or block transfers
  - fully interlocked, blocking, single word or block transfers
  - variable depth FIFOs



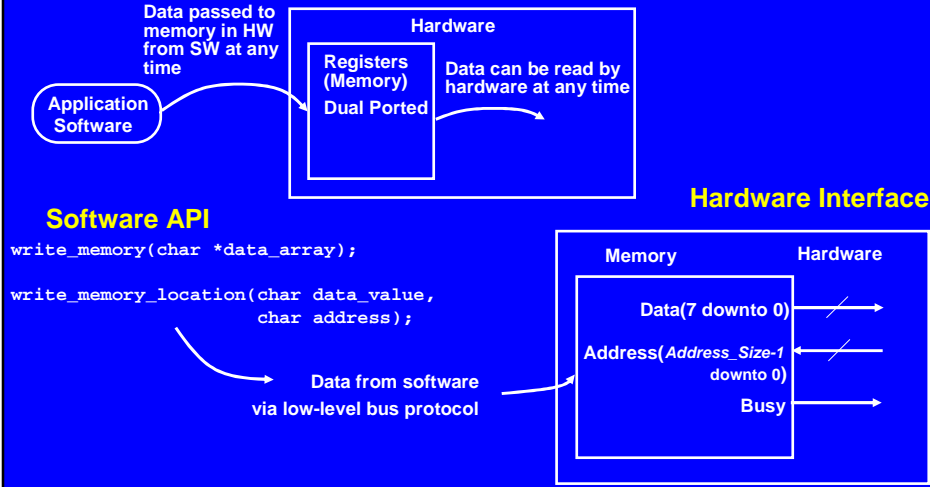
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# Hardware/Software Communications Library



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## Asynchronous memory-mapped HW to SW data transfer



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# The Future Implementation Platform- the MERCAL



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- MERCAL - Miniature Embedded, Reconfigurable Computer and Logic
- Project sponsored by NASA to develop a small, powerful, low-cost, easily programmed, reconfigurable hardware/software system
- Hardware is based on Xilinx, Spartan II FPGAs
- Software is based on JumpTec sub credit card sized DIMMPC
- The MERCAL final version of the MERCAL boards are being developed at VCU this summer and will form the basic HW/SW system for future projects

DIMMPC

Xilinx Spartan FPGA





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# The MERCAL is Here



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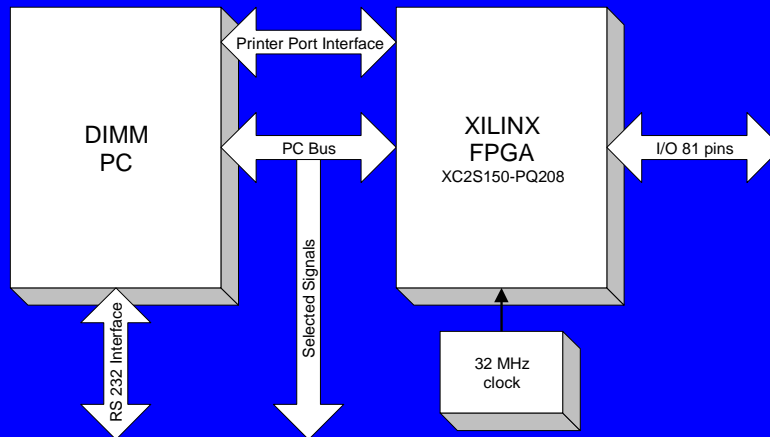


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# MERCAL Architecture



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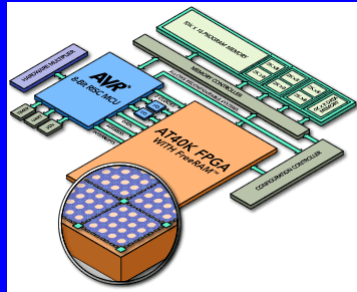
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# Alternate HW/SW Platforms

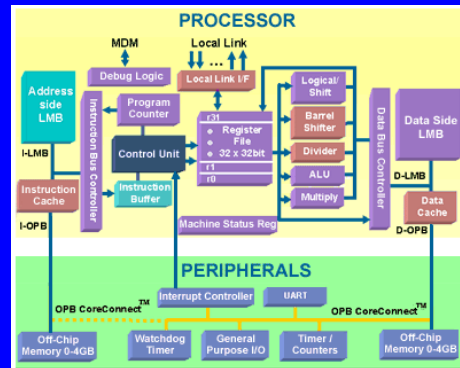


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## Actel FPSLIC



## Xilinx Microblaze



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# The 2003 Project – the Skybot



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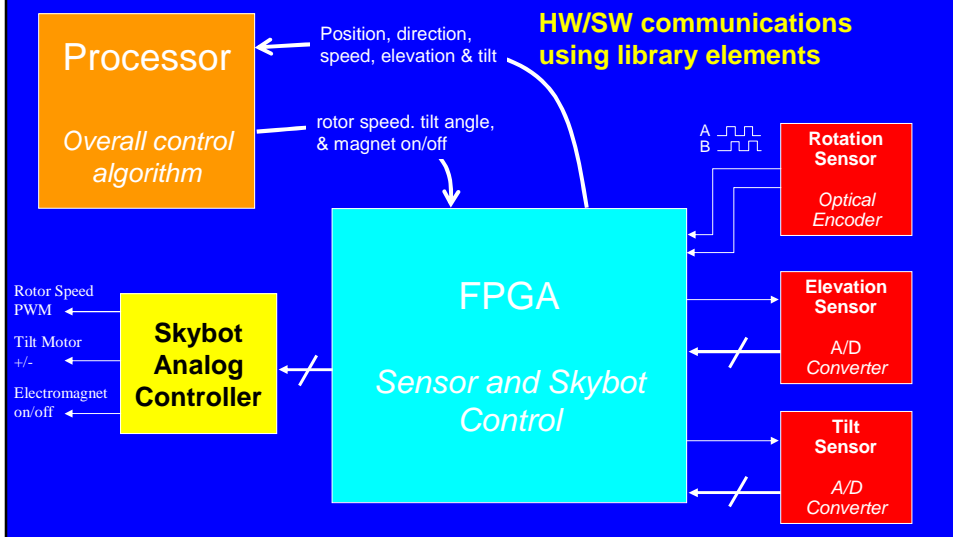


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# Skybot - Typical System Architecture



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# Skybot - Results



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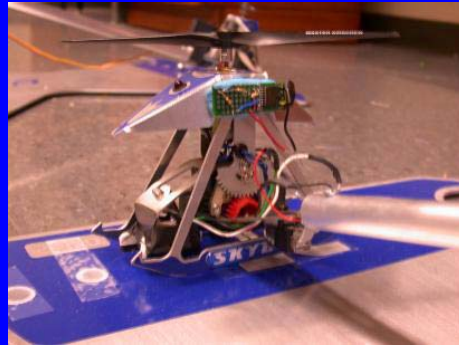
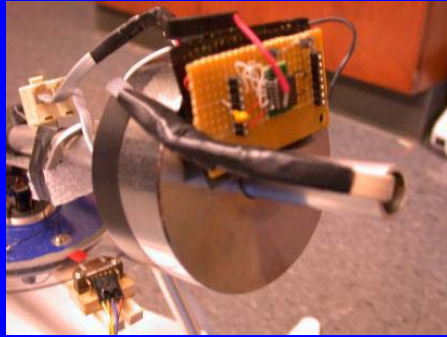


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## Skybot – Results (cont.)



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## Skybot – Results (cont.)



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## Conclusions



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- Not enough simulation with Xilinx devices
  - creating and downloading a new bit file was “easier” than constructing a thorough test bench for simulation, but
  - hardware problems are difficult to diagnose in the FPGA (no observability)
  - ex; one group spent 3 days trying to track down and fix a problem that the instructor was able to diagnose after about an hour spent constructing a test bench and the fix took less than 15 minutes to implement and test
- “NIH” syndrome for interface components
  - when the hardware didn’t work or returned values the students didn’t expect, they tended to place the blame on the part of the design they didn’t implement and didn’t understand
  - NONE of the problems encountered turned out to be a problem with the interface components
  - lack of simulations tended to compound this problem



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## Conclusions (cont.)



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- Student’s software design skills are weak - especially in the area of real-time control
  - code tended to be a sequential series of steps without feedback
  - experience and skill in dealing with I/O routines also was lacking
- Material described herein is available
  - see student papers in the poster sessions for a description of PBMT and the communications library
    - PBMT available now
    - MERCAL version of the communications library completed
  - implementation of the communications library for FPSLIC will be completed by the end of the summer
  - web site coming in the next month
    - <http://www.people.vcu.edu/~rhklenke/ccli>
  - email the author
    - [rhklenke@vcu.edu](mailto:rhklenke@vcu.edu)