



## VALID: Custom ASIC Verification and FPGA Education Platform

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## Overview

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- What is VALID?
- Overview of the VALID Design
- VALID Hardware
- VALID Software
- Possible Applications
- Future Work



## VALID History

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- 2001 - Student PCB Design Project
- 2003 - Improving Courses
- VALIDx1: Lattice CPLD Interconnect
- VALIDx2: Xilinx CoolRunner CPLD
- VALIDx3: XCV1000, ETRAX Microprocessor



## What is VALID?

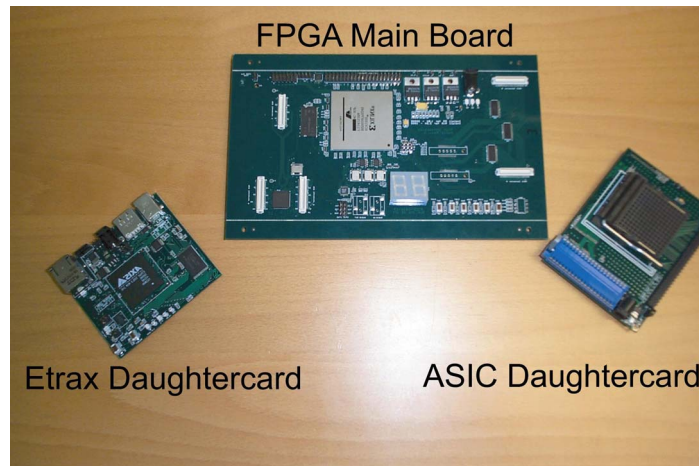
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- VALID: VLSI AASIC Logic-analyzer Interface Design
- Designed Entirely at Rice University
- Third Generation of VALID Hardware
- Functional Verification of Custom ASICs
- General Platform for Teaching FPGA Design and Implementation

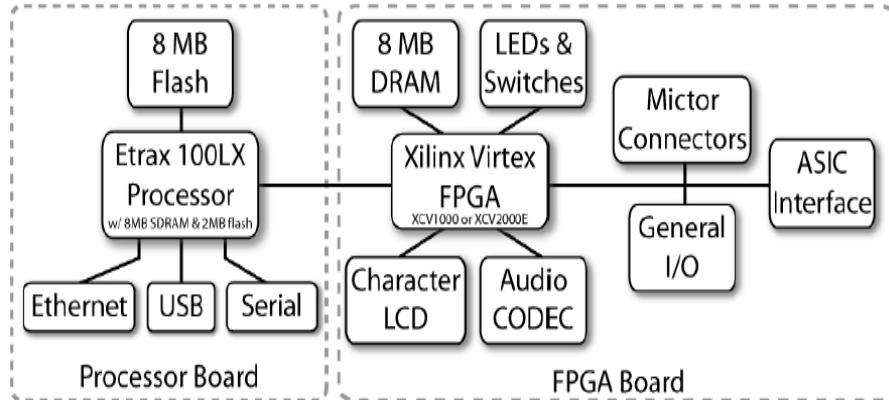
## Motivation

- Universities Typically Lack Low Cost Platforms for Custom ASIC Verification
- Previous Hardware Relied on External Logic and Breadboard
- Desired FPGA Command Line Configuration
- Desired an Interface Between a FPGA and the ETRAX Microprocessor
- Implementation of Simple ASIC Verification Platform

## VALID Hardware



## VALID Hardware

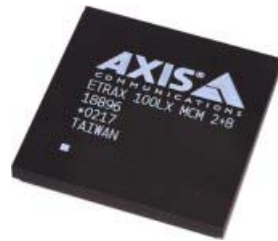


## VALID Hardware Overview

- Axis Etrax 100LX Microprocessor
- Xilinx Virtex FPGA
- Peripherals and External Interfaces to Increase Educational Possibilities
  - LCD Character Display
  - Audio Codec
  - On Board SDRAM
  - High Speed Serial
  - USB 1.1
  - 10/100 Ethernet

## Axis ETRAX 100LX

- 100 MIPS RISC Processor
- Designed to Run Linux Which Greatly Simplifies Software Design
- Multi-Chip Module Simplifies Board Design
  - Etrax Core
  - 10/100 Ethernet interface
  - Flash Memory – 2MB
  - Integrated SDRAM – 8MB



## Xilinx Virtex FPGA

- Virtex XCV1000 FPGA
- Any Virtex or Virtex-E FPGA Supported
- Selectmap Configuration Mode, Fastest Configuration Mode
- 16-Bit Memory Bus at 50 MHz
- High Datarate Allows for
  - Large Bandwidth Between ASIC Under Test and Etrax MCM
  - For Complex Real-Time Signal Processing Designs Within the FPGA



## VALID Infrastructure Software

- Data Exchange Between the Etrax and the FPGA
- Written in C, Cross-Compiled to Etrax Processor
- Etrax Treats the FPGA as Asynchronous Memory Device
- Allows for Memory Access Code to Gracefully Communicate with the FPGA



## VALID User Interface Goals

- Simulink and Labview Support in Real-time
- Simulink Offers an Intuitive Environment for both FPGA Design and ASIC Verification
- Possible to Completely Control VALID via Widely-Used Telnet



## VALID as Educational Platform

- XCV1000 Allows for Larger Designs Than Other Basic and Intermediate FPGA Boards
- Needs Only a Bitstream Via FTP or NFS to Configure FPGA
- Flash Memory is Large Enough to Hold Multiple Bitstreams
- Provides Multitude of I/O Peripherals for ASIC Verification

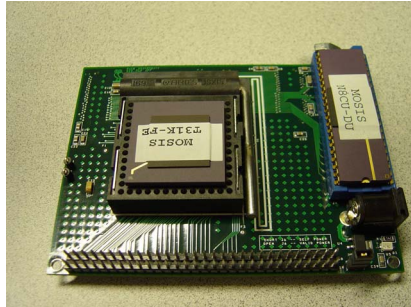


## VALID as Educational Platform

- Current Course Use
  - Elec 422/423 – ASIC Verification
  - Elec 522 – FPGA Implementation
- Planned Course Use
  - Elec 327 – Digital Logic Design
  - Elec 430 – Digital Communications
  - Elec 437 – FPGA Embedded System Design

## Ongoing Projects

- ASIC Verification
- FPGA Implementation



- GigaBit Network Card
- Ethernet Configuration of FPGAs
- Multiple Use FPGA System Integrated into VLSI, DSP, and Communications Curriculum

## Acknowledgements

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