

# Teaching Bus Architectures with a Basic, Hands-On SOC Platform

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- Course: INF6501
- Evolution of the Platform
- Applications
- Results
- Improvements

# INF6501: Curriculum

## Specification and Design of Embedded Systems

- Embedded System Architectures
- System Specification (abstraction)
- Architectural Exploration
- System Synthesis
- Verification Concepts and Tools

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# INF6501: Objectives

## **Specification:**

- Present high-level description languages
- Develop a concrete understanding of system architectures.

## **Design:**

- Teach architecture exploration techniques
- Encourage design reuse

*How do we attain these objectives in the lab?*

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## INF6501: Objectives (cont)

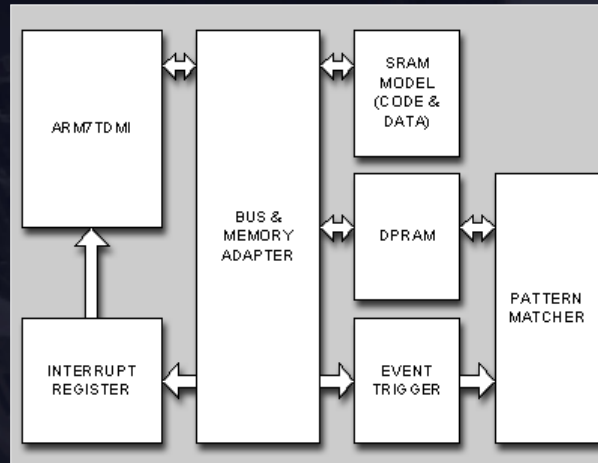
### Conclusion:

- The use of a **VHDL model of a platform** in a lab assignment allows the student to attain the objectives

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## Evolution: Old Structure



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## Evolution: Problems

- **Difficult to add or remove modules:** requires extensive modification in several components
- Bus architecture dependent on the ARM7's **pinout** and **behaviour**

*What can we do about it?*

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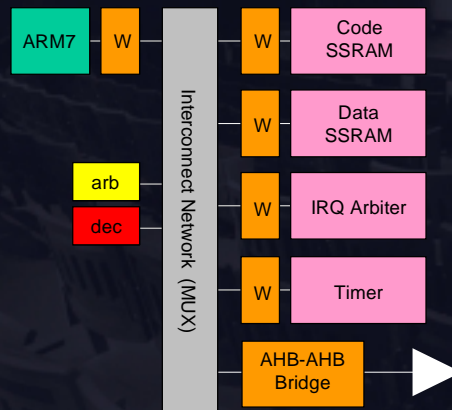
## Evolution: Bus Protocol

- A bus protocol can improve the situation by providing a **bus structure** and a **standard interface**
- Module interfaces are **converted** using **wrappers**

## Evolution: AMBA Bus Protocol

- We chose the AMBA AHB bus protocol for use in our platform
- It **proposes** a bus architecture that is well documented and widely used
- It allows the students to understand the notions of **masters, slaves, arbiters, decoders** and **bridges**

## Evolution: Current Structure



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## Applications: Tools

- CAPTURE : HDL Designer Pro
  - Strong learning curve
  - GUI improves understanding of system
- VERIFICATION : Seamless CVE
  - Adds flexibility to debugging by allowing the designer to place breakpoints in both HW and SW code

## Applications: Environment

- The students download the lab material (HDP files)
- Seamless CVE configuration files are already supplied

## Applications: Module Design

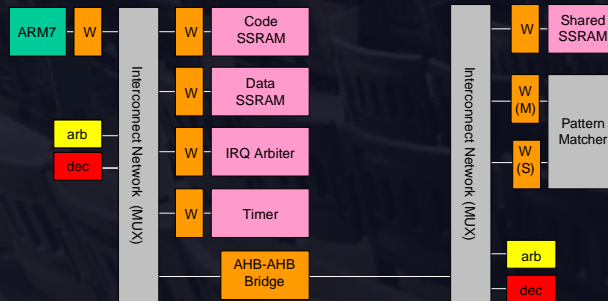
- Lab1, winter 2003: add a timer and wrapper to a simplified version of the platform
- Knowledge gained:
  - AHB architecture and slave interface
  - Wrapper design

## Applications: C-Bridge

- Lab 3, winter 2003: Add a pattern matching module, coded in SystemC
- Knowledge gained:
  - The use of a high-level language to verify a concept before implementing it
  - Understanding of C-Bridge, a function of Seamless that allows a mix of SystemC and VHDL

## Applications: Pattern Matcher

- Similar to lab 3, but entirely in VHDL
- Used for a Seamless tutorial



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## Results: Learning Curve

- Keep labs simple: 80% of the allotted lab time is used to understand the platform, the tools and the protocol
- The protocol has to be summarized into a set of rules to respect:
  - ‘ignore access if HTRANS=00’
  - ‘activate WR signal if HWRITE=1 and HSEL=1’

## Results: Subject Matter

- Students moderately to very satisfied
  - Hands-on, low level, realistic situation
- Would have appreciated code samples
  - Use other wrappers in design as examples
- Would have wanted a greater understanding of the AMBA protocol
  - At what price?

## Results: Difficulties with Tools

- Some debugging tools were rarely used (especially the software debugger)
- Students mainly used chronograms & breakpoints, but made little use of variable examiners
- For some, HDP takes too long to learn for a single lab

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## Improvements: Adding OCP

- Although the new platform is more flexible and reusable, flexibility could be improved
- OCP, based on the VCI effort, can reduce the number of wrappers a designer has to make for a given IP module

## Improvements: Delays

- Focus is directed towards the causal relations between the signals
- The designs are not checked for timing constraints
- Synthesis will give a more realistic evaluation

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