



UNIVERSITY of NEW HAMPSHIRE

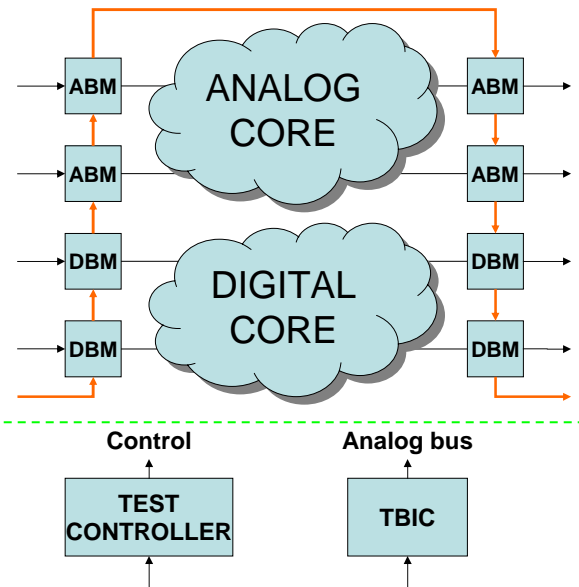


A DOT1 & DOT4 Mosis - Compatible Library

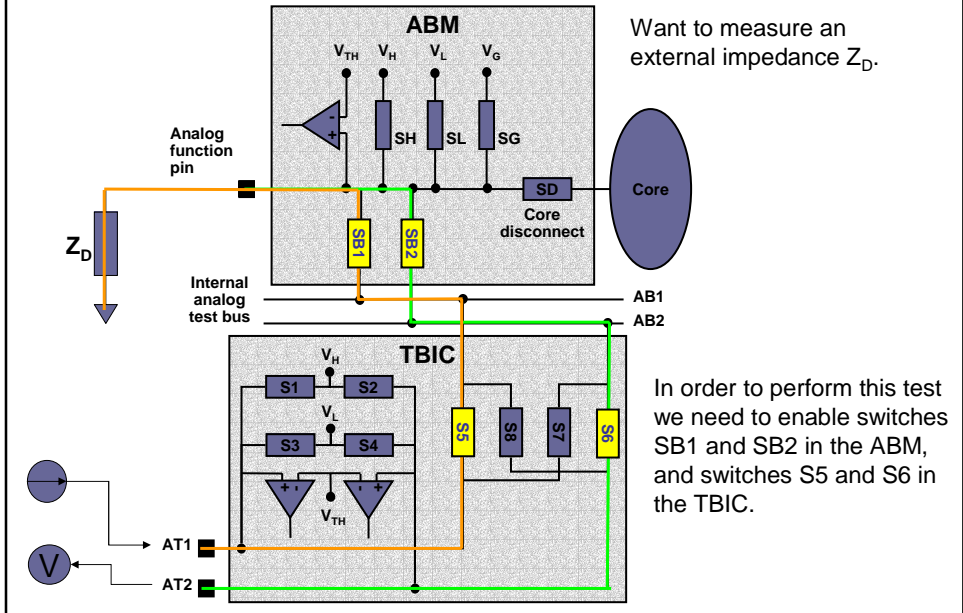
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Barrett Stetson, and S.T.P. Brundavani*

<http://www.ece.unh.edu/courses/ece715/>

IEEE 1149.4 Overview

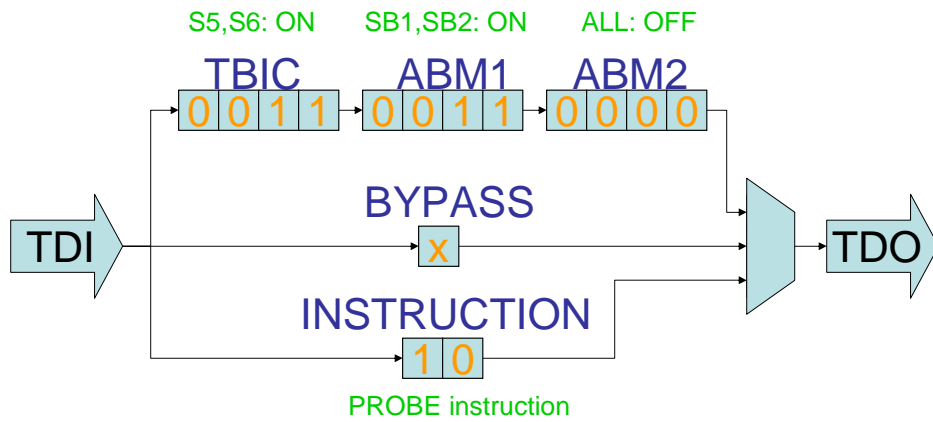


Simple Test Scenario

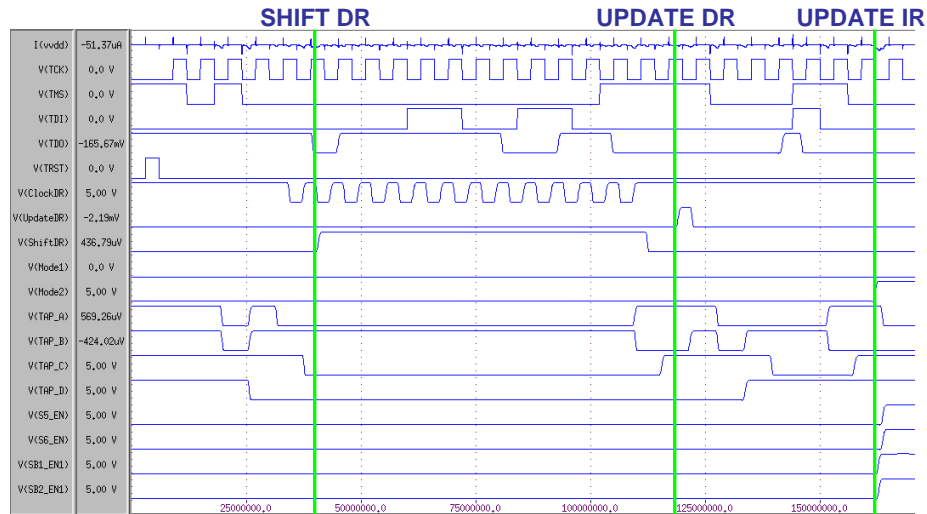


Setting up the Test Scenario

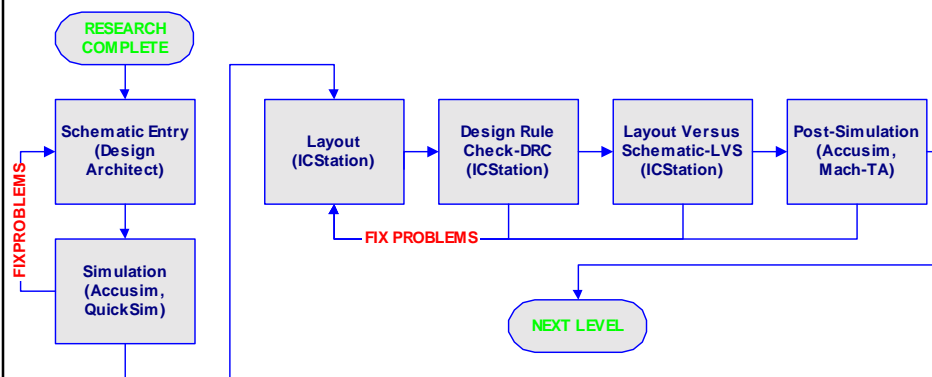
Switch states depend on control signals configured locally to the TBIC and ABM as well as the current instruction.



Simulation Results

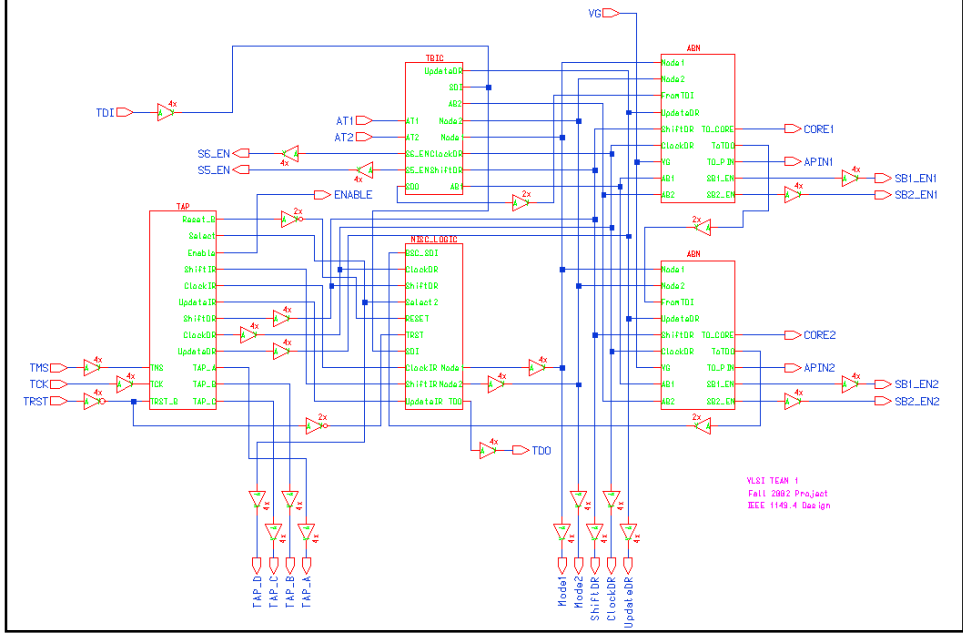


Design Process

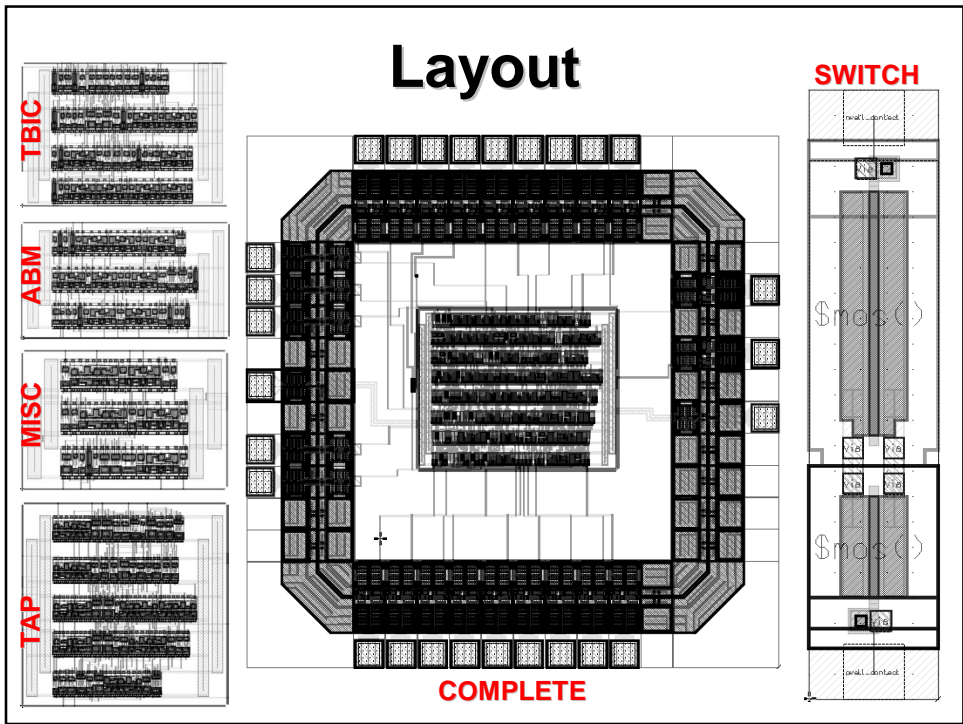


This is the basic design process used in creating the modules of the project. After each module was completed a similar process was used to create the top level design.

Top Level Schematic

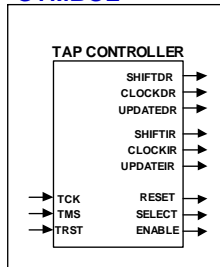


Layout

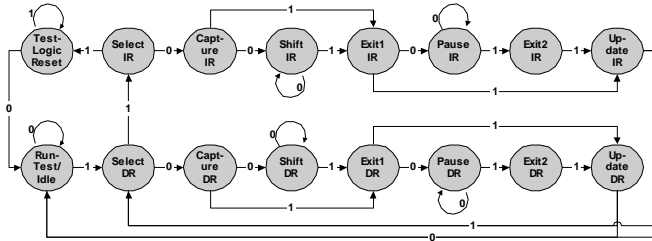


TAP Controller

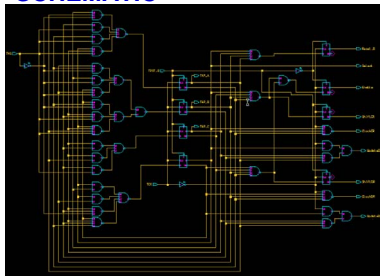
SYMBOL



STATE DIAGRAM



SCHEMATIC



LAYOUT

