

On simulating the IP Market Dynamics in an Academic Environment Using SystemC

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Overview

- Purpose:** Teach engineering students hierarchical system design with SystemC; Integrate impact of market dynamics & entrepreneurial ideas
- Method:** CAD based computer design class using SystemC™ that integrates digital design engineering with marketing principles
- Result:** Appreciation of cross disciplinary experiences required for graduating engineers of today



Introduction

- A semester long undergraduate CAD Based Computer Design course
- 52 undergraduate students + 3 teaching assistants
- SystemC™ taught at the RT Level
- Provide real-life experience of IP (intellectual property) development and integration



Introduction...

The simulated IP market had 3 major participants

- *IP developers* : Developed basic building blocks (IP) for digital design
- *EDA Vendors* : Primary objective was to rank these IP blocks on a scale of 1 to 5
- *System Designers* : Selected the better ranked IP blocks to integrate and model their systems. Selection matched the rankings



SystemC™

- Open Source HDL (hardware description language)
- Enables system and RT level design and IP exchange
- C++ based modeling language
- Flexibility of compiling on any standard IDE that supports C++ (Visual Studio)
- Available for download from www.systemc.org



Methods

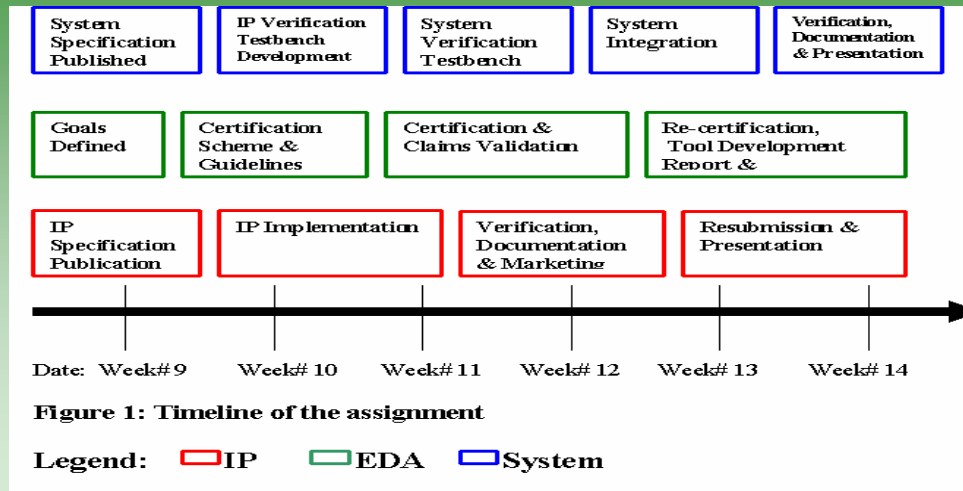
3 Course Assignments

- First assignment focused on giving students hands-on simulation and verification experience using SystemC™
- Second assignment, a half semester long project, focused on the simulation of IP market dynamics
- Third assignment focused on the design of a finite state machine using SystemC™



Methods...

Assignment 2: Simulation of IP market Dynamics



Methods...

- 16 IP Companies
- 4 EDA companies
- 6 System Companies
- Each company had 2 members (students)
- Each group of companies had an assigned mentor (teaching assistants) to guide them
- Most students chose their roles



Methods...

1. System Companies publish their design specs in English and posts them on the company website
2. IP companies inspect these specifications and choose a pair of IP blocks to design
3. IP companies publish their specs online
4. IP companies begin implementing their design in SystemC™ and provide documentation online.
5. After the implementation stage, IP's are tested using drivers and monitors written in SystemC™



Methods...

6. IP companies then develop an application note which includes all or some of the following
 - Block Diagrams
 - Schematics
 - Source code for the designs including drivers and monitors
 - Examples of usage
 - Any other pertinent information about their IP



Methods...

7. EDA develop potential drivers and monitors for the IP blocks. The rankings are based on a scale of 1 to 5, 5 being the best
 - 1 point for adherence to coding guidelines
 - 1 point for functional accuracy;
 - 1 point for implementing the IP with at least one of the following
 - Hierarchical design
 - Low power design
 - Low delay
 - Reduced gate count
 - 1 point for application notes

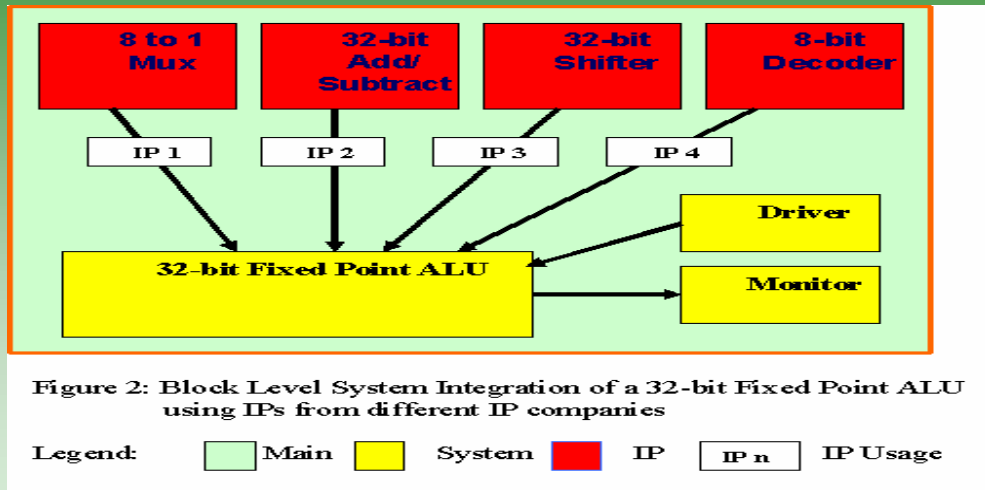


Methods...

8. EDA companies also try developing tools or flows to automate some of the design process
9. IP companies that scored poorly on the rankings are given a second chance to improve their IP blocks and have them recertified. But good IP companies are already in dialog with System companies.
10. System Companies pick their IP partners. EDA companies' rankings help, but direct communication matters. The IP from companies are picked and integrated to meet the specs (EDA rankings validate the selections).



Methods...



Results & Discussion

- Students with software background had difficulty with hardware concepts like concurrency & signals
- Students with hardware background had difficulty modeling hardware elements in C++
- EDA companies had difficulty in developing drivers and monitors since the structural details (port types, signal types) of the IP were not known in advance



Results & Discussion...

- Debugging of the system during the integration phase was difficult
- Debugging at system level also took a considerable amount of time when compared with IP development & debugging
- Verification and documentation took up the 'slack' non-design time



Results & Discussion ...

- IP Companies prepared a rich set of deliverables
- Good IP companies finished early, worked closely with System companies, and helped them integrate.
- EDA companies worked very closely with IP companies to verify the claims
- The grading policy for this assignment was very relaxed since
 - Innovative exploration could be promoted
 - Students were unfamiliar with such non traditional assignments



Conclusion

- This course combined IP market dynamics with SystemC-based digital design
- This course also allowed students from different backgrounds (computer science and computer engineering) to participate in a simulated market environment which was conducive for an enhanced cross-disciplinary experience



Links & References

- [1] International Technology Roadmap for Semiconductors: <http://public.itrs.net> , 2002
- [2] Keating, M., and Bricaud, P., *Reuse Methodology Manual*, 3 rd edition, Kluwer, 2002
- [3] Virtual Socket Interface Alliance (VSIA): <http://www.vsi.org/>
- [4] Chang, L., et al., *Surviving the SOC Revolution*, Kluwer, 1999
- [5] Grotker, T., et al., *System Design with SystemC*, Kluwer, 2002
- [6] The Open SystemC Initiative: <http://www.systemc.org/>
- [7] Gajski, D.D., et al., “Essential Issues for IP Reuse”, *Proceedings of the ASP-DAC 2000, Asia South Pacific* ,pp. 43-48, 2000
- [8] Bhasker, J., *A SystemC Primer*, Star Galaxy Publishing, 2002
- [9] Our Center’s webpage for the keyed samples: <http://www.cvsf.fau.edu/systemCexamples>

