The Sandbox Design Experience Course

Using Network-on-a-Chip in a Collaborative, Multi-University Design Course

Herman Schmit, Thomas Kroll, Max Khusid (CMU)
N. Vijaykrishnan (Penn State)
Ivan Kourtev (Univ of Pittsburgh)
Dave Landis (Pittsburgh Digital Greenhouse)

http://www.ece.cmu.edu/~ece725

Difficulties with VLSI Design Classes

- Using Industry Standard ASIC Design Flow
  - SupportingTool/Library Infrastructure

See Companion Poster on Digital Sandbox

- Creating Project Specification
  - Interesting, Challenging, Relevant
  - Possible to complete in one semester

- Techniques to:
  - Partition Design Effort
  - Reduce Interdependences
  - Enforce Reasonable Interfacing
  - Enforce Testbenching

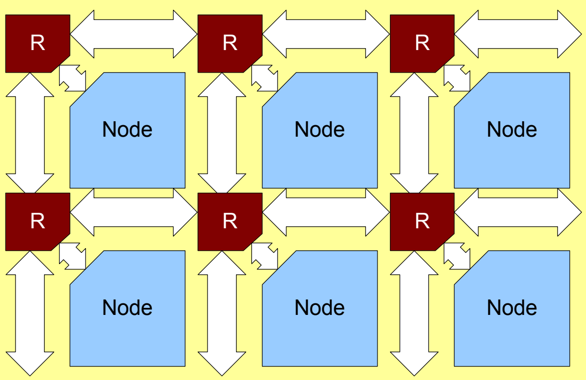
This Class Solves These Problems Using Network-on-a-Chip Methodology

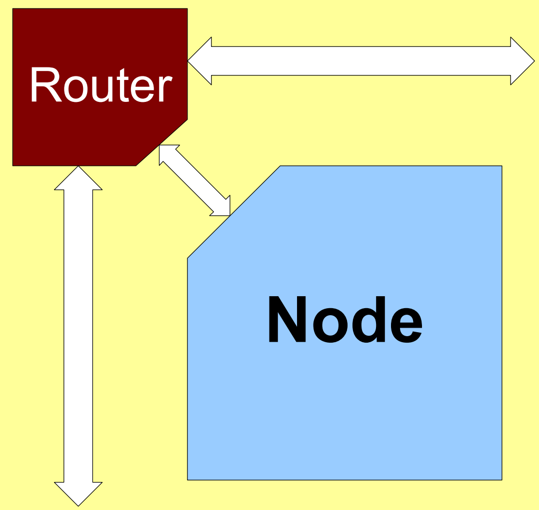
Network on a Chip

- Separate System Spec into different interacting **Nodes**
  - Implement each Node as “little ASIC”
  - Can be different or the same, depending on application

- Connect components using:

  Dynamically Routed, Packet Switched Network
- Implement Network using a mesh of **Routers**





- **Advantages:**
  - Manageable Node Size
  - Pre-defined Interfacing
  - Fewer Dependencies, Better Testbenching

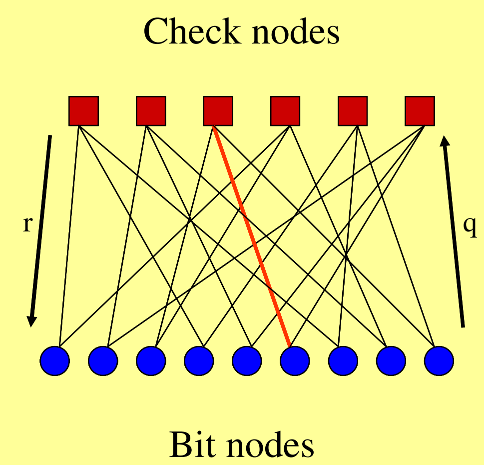
The Application

- Requirements:
  - Well-Defined
  - Interesting, Relevant to Industry
  - Partitionable into Network-on-a-Chip Methodology

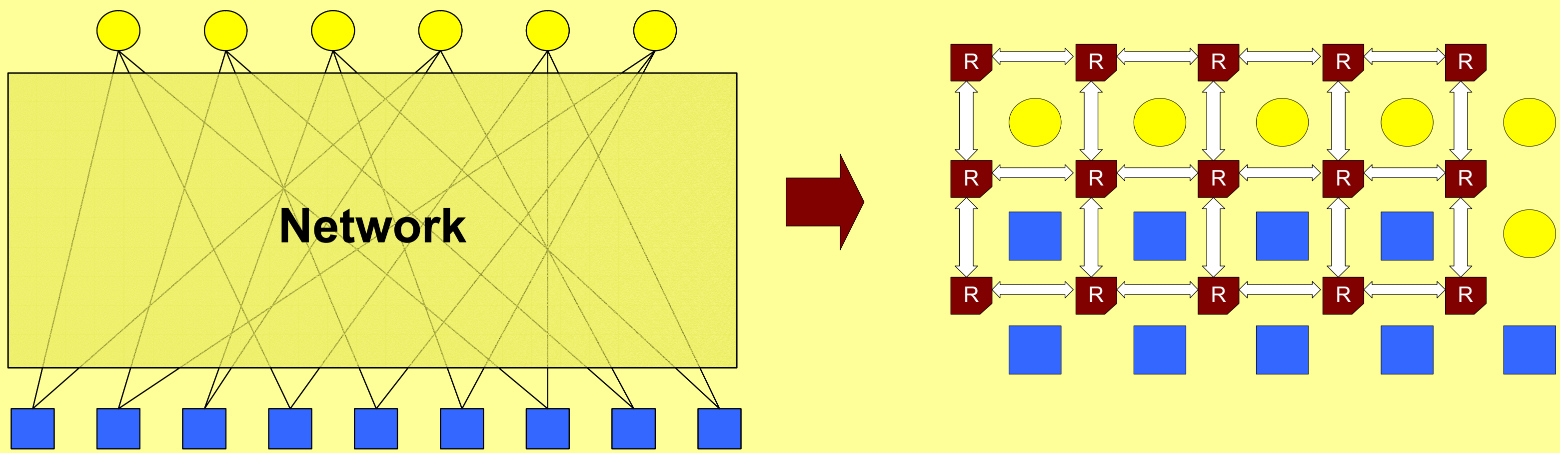
- **Low Density Parity Check Decoders**
  - Relevance:
    - Near-Shannon Limit Performance
    - Interesting for Wireless, Network & Storage Markets
  - Decoding Algorithm:
    - Iterate on Bi-Partite Graph of “Bit Nodes” and “Check Nodes”

1	0	0	1	0	0	1	0	0
0	1	0	0	1	0	0	1	0
0	0	1	0	0	1	0	0	1
1	0	1	0	0	0	0	1	0
0	0	0	1	0	0	1	0	1
0	1	0	0	1	1	0	0	0

Parity check matrix, H



LDPC and N-o-C



- Use Network to Provide Bi-partite Inteconnection
- Different code → Different Routing

- Objectives:
- Make it Programmable: Any H Matrix
- Make it Capable of Dealing with Big Block Codes: Virtualize

Class Schedule

- Two Big Phases:
  - Phase I: Small Labs to Acquire ASIC Design Skills
  - Phase II: Design LDPC decoder using NoC

- Prerequisites:
  - Some Basic VLSI (Digital Circuits) and Layout
  - C, Perl, Verilog
  - No Assumed Familiarity with ASIC Design Flow

<u>Phase I:</u>

- Lab 1: RTL Design and Tesbench (2 weeks)
  - Design a FIFO Interleaver, Build a Testbench
  - Use Design Assertions (Open Verification Library)
  - Swap Design and Testbench with a random peer

- Lab 2: Synthesis (1 week)

- Lab 3: Physical Design (1 week)

} These are Cookbook

Phase II

- Break into Teams: Each Team Designs Complete Decoder
  - Three Universities → Four Teams
  - 2 @ CMU, 1 @ PSU, 1 @ Pitt

- Break each Team into Subteams:
  - Check Node Team
  - Bit Node Team
  - Router Node Team

These Teams do RTL and Component Testbenches

  - Architecture and System Verification Team

Architecture Team determines:

Network Parameters

Interface Parameters

Number of Nodes

Placement of Nodes in Network

Builds System Verification Testbench

Multi-University Collaboration

- Three Administratively Separate Courses
- Same Phase I, Phase II Timing
  - Problem: Pitt Opens early, closes early

Phase II: Design Reviews

- Two Incremental Design Reviews (1 Week Each)
- One Final Design Review (2 Weeks, 4 Class Sessions)
- Presentations Shared Using WebEx
- All Four Parallel Subteams give participate in design review

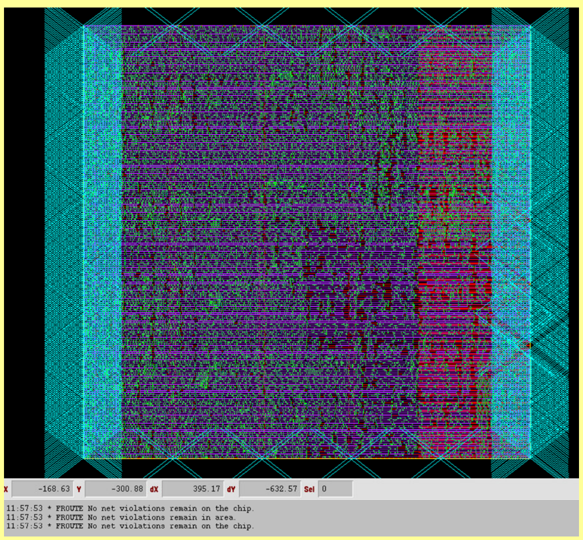
- Parallel Sub-Teams: **Collaborative/Competitive Dynamic**
  - Corresponding Sub-Teams are designing to the same spec
  - Extremely Knowledgable Audience at Design Reviews
  - Students learn about diversity of approaches
  - Students learn to be critical of other designs, helps with own
  - Concept of Balanced Design

Outcomes I

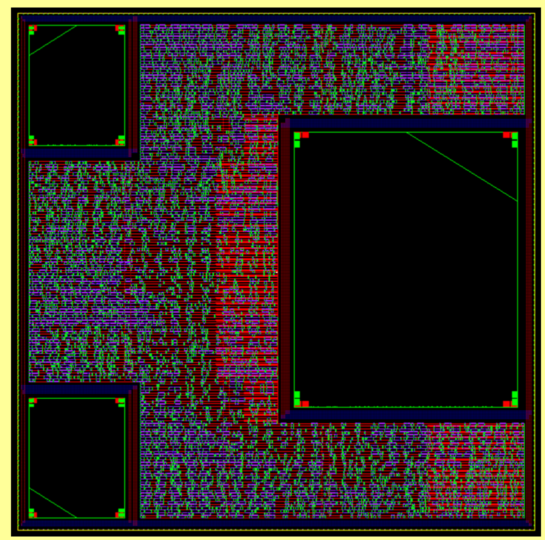
- Teams Completing RTL (4/4)
- Teams Completing Chip Testbench (2/4)
- Teams Meeting Design Goal (3/4)

> 1Gbps/iteration and < 100mm2

- SubTeams Completing Unit Testbench (8/12)
- SubTeams Completing Synthesis (12/12)
- SubTeams Completing Place/Route (9/12)



965 sq. microns, 88% utilization



965 sq. microns, 44% utilization