

Performance-Based System Design Education

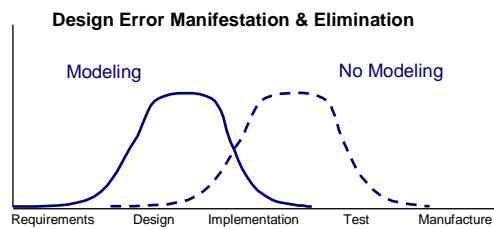
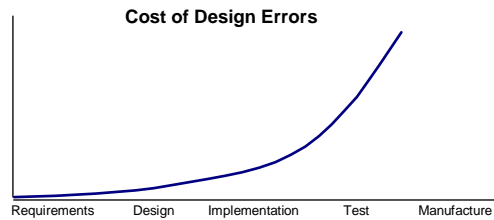
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Project Overview

- ▶ Performance Based Modeling Tool
- ▶ Explore design alternatives by estimating performance of high level abstract model
- ▶ Task graph behavioral model mapped to an architecture
- ▶ Prefabricated architecture library modeled in SystemC
- ▶ Simulation provides performance statistics
- ▶ Simulation creates an execution timeline

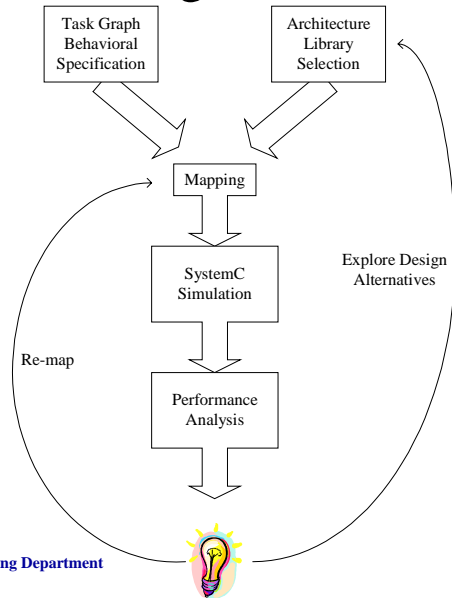
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Benefits of Performance Modeling



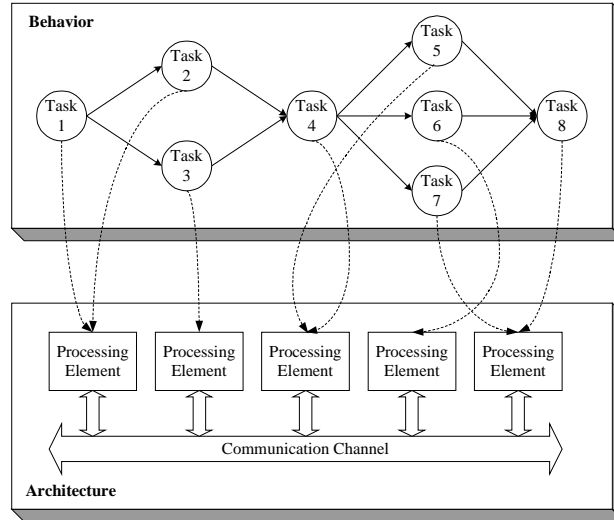
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Design Flow



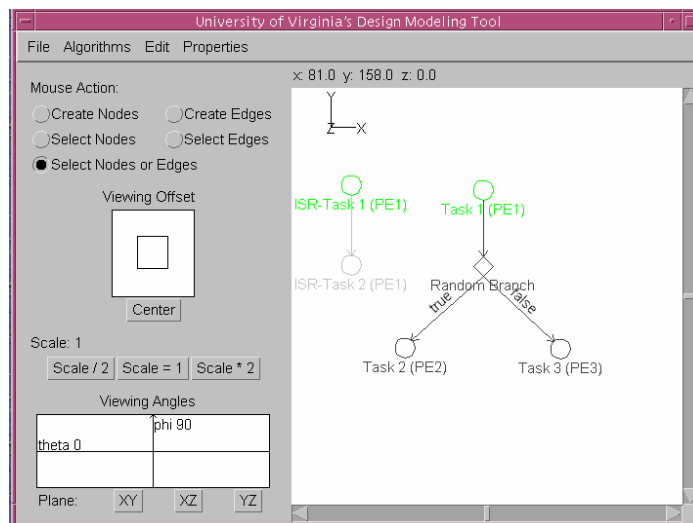
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Mapping



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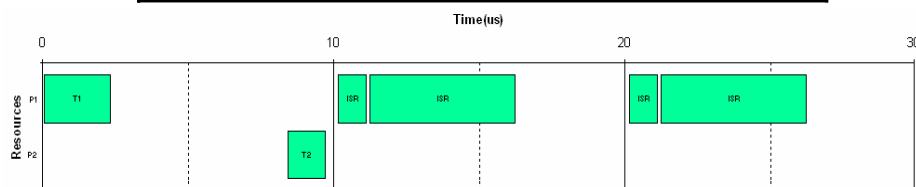
Task Graph Interface



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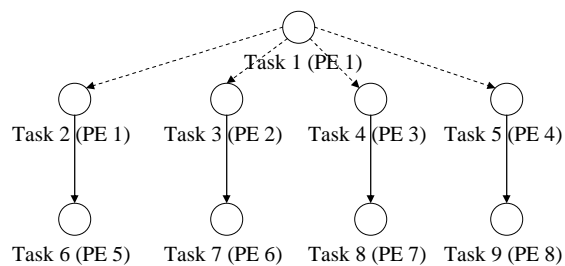
Statistics and Execution Timeline

Throughput	.0667 tasks/ μ s
Latency	9.75 μ s
Utilization	PE1: 28% PE2: 25%
Compute Utilization	PE1: 8% PE2: 4.5%
ISR Utilization	PE1: 40% PE2: 0%



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Design Alternatives



Architecture	Latency (μ s)
Shared Channel	45.95
Crossbar Switch	35.75
Fully Connected	30.85

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