



**LUND**  
UNIVERSITY

# Teaching Digital HW-Design by Implementing a Complete MP3 Decoder

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## Course facts

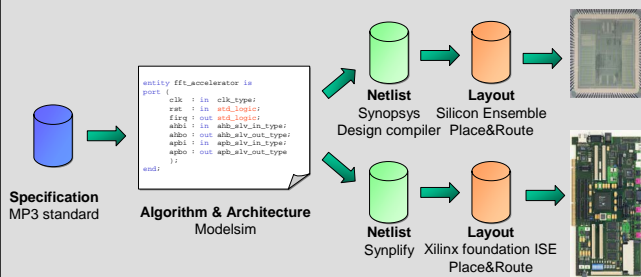
**Course name:** IC project and verification

**Prerequisites:** Digital IC design

**Duration:** eight-week full time

## Course outline

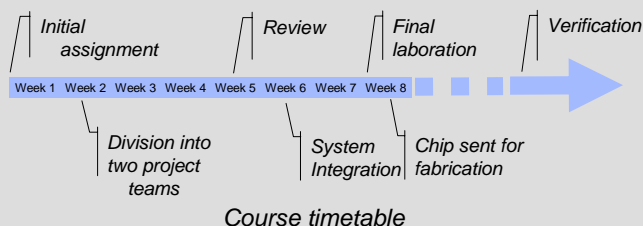
- Design and analysis of MP3 submodules
- Simulation and debugging of HDL code
- CAD tools for synthesis and place & route
- System integration
- To show the importance of a design flow
- Two major tracks: ASIC or FPGA



Design flow used during the course

## Project description

- I. Initial assignment in groups of two students
- II. The groups are divided into two project teams, each implementing a complete MP3 decoder
- III. One of the implementations is sent for fabrication



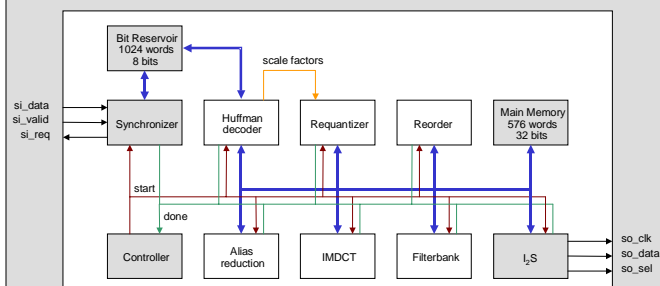
Course timetable

## The students are provided with

- Reference model in C and project manuals
- VHDL block-interface description and testbench
- Tutorials and scripts for the CAD tools

## MP3 facts

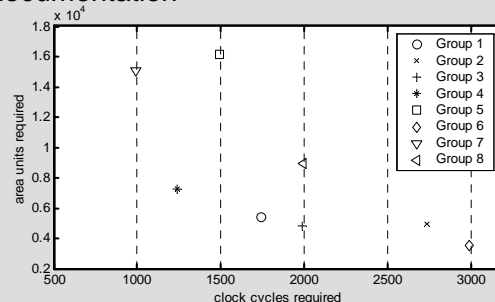
- Removes 90% of the information with no significant audible impact
- Combines perceptual and lossless coding schemes



MP3 decoder architecture, shaded boxes are provided as VHDL IP-blocks to the students

## Important factors to motivate the students

- Implementation of a widely used standard
- Working in groups towards a common goal
- Regular meetings with the supervisors
- Feedback on synthesis results, code and documentation



Synthesis result from the initial assignment

## Results

- ASIC in 0.35  $\mu\text{m}$  process (21 mm<sup>2</sup>)
- FPGA implementation 59% of Xilinx XC2V1000

