

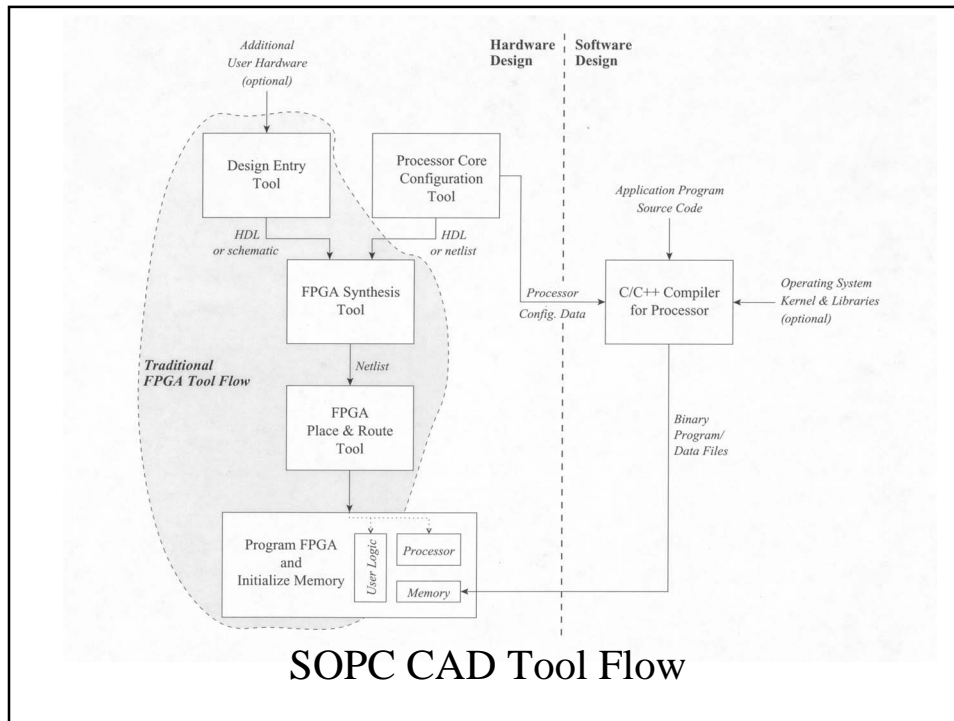
Using an FPGA-based SOC Approach for Senior Design Projects

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OVERVIEW

- An FPGA-based SOC development board with a soft RISC processor IP core is used to support undergraduate design projects.
- Commercial CAD tools, a C compiler targeted for the RISC processor IP core, and a large FPGA are used in the tool flow.



SOFT PROCESSOR CORES

Feature	Nios 3.0 (Altera)	MicroBlaze 3.2 (Xilinx)
Datapath	16 or 32 bits	32 bits
Frequency	up to 150 MHz ¹	up to 150 MHz ¹
Gate Count	26,000–40,000	30,000–40,000
Register File	up to 512 (window size: 32)	32 general purpose and 32 special purpose
Instruction	16 bits	32 bits
I-Cache	Optional	Optional
Multiplier	Optional	Optional
Pipeline	5 Stage	3 Stage

¹This speed is not achievable on all devices. Some devices limit the maximum frequency to as low as 50 MHz.

EXAMPLE STUDENT PROJECTS

- Examples of student projects include internet appliances, mail servers, vision systems, and robots.
- Additional FPGA logic used for extra I/O hardware such as serial ports and PWM control for servos



R/C Hummer with NIOS SOC board and CMUCAM.
Extra FPGA logic was used for servo PWM
controllers.



Amigobot controlled by NIOS SOC board. Extra FPGA logic was used for serial ports, sensor interfaces, and an LCD interface.